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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,935	03/19/2004	Shinichiro Shiratake	250798US2S	6721

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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 04/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/803,935	SHIRATAKE ET AL.
	Examiner	Art Unit
	Thong Q. Le	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-16 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-16 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-16 are presented for examination.

Information Disclosure Statement

2. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 08/09/2004.

3. Information disclosed and list on PTO 1449 was considered.

Priority

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 9-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. The term "third and fourth bit lines" in claims 9-13 are is a relative term which renders the claim indefinite. The term "third and fourth bit lines" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

The "third and fourth bit lines" are not defined in specification. Refer to Figure 13 of application, examiner understand that invention including two of memory cell array Left and right, and they shared common amplifier S/A.

Reference Takashima discloses a sense amplifier can be shared by the memory cell arrays on opposite sides for saving space (column 10, lines 65-67) as presented invention discloses.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000.

Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

10. Claims 1-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Takashima (U.S. Patent No. 6,549,449).

Regarding claims 1, Takashima discloses a semiconductor integrated circuit device (Figure 17) includes a series connected TC unit type ferroelectric (MA) RAM which includes series connected memory cells each having a transistor having a source terminal and a drain terminal and a ferroelectric capacitor inbetween the two terminals, the device comprising:

first and second bit lines (/BL, BL);

first and second plate lines (/PL, PL) ;

a first series connected TC unit (C1) type structure which includes series connected memory cells, and has one terminal connected to the first bit line via a first selection transistor and the other terminal connected to the first plate line (Figure 17) ;

a second series connected TC unit type structure which includes series connected memory cells, and has one terminal connected to the second bit line via a second selection transistor and the other terminal connected to the second plate line (Figure 17) ;

word lines (WL) connected to gates of the series connected memory cells included in the first series connected TC unit type structure and gates of the series connected memory cells included in the second series connected TC unit type structure;

a plate line potential control circuit (Figure 17, PL Driver) which controls, in a standby state, potentials of the first and second plate lines to a first potential and, in an active state, the potential of the first plate line from the first potential to a second potential and the potential of the second plate line from the first potential to a third potential when one of the series connected memory cells included in the first series connected TC unit type structure is selected; and

a bit line potential control circuit (ABSTRACT) which controls a potential of the second bit line the third potential, after charges are transferred from one of the ferroelectric capacitor included in the first series connected TC unit type structure to the first line (Column 3, lines 53-67, column 4, lines 1-28).

Regarding claims 2-9, Takashima discloses wherein the plate line potential control circuit controls the potential of the first plate line from the second potential to the third potential, after controlled to the second potential (Column 4, lines 65-67, Column 5, lines 1-40), and wherein plate lines except the first and second plate lines maintain the first potential in the active state (column 5, lines 1-5), and wherein the bit line potential control circuit controls a potential of the first bit line to the third potential, after charges are transferred from one of the ferroelectric capacitor included in the first series connected TC unit type structure to the first bit line (Column 5, lines 1-40), and an amplifier (Figure 17, S/A) which uses the charges transferred to the first bit line as a signal and the second bit line as complementary bit line and amplifies the signal, and further comprising a switch (Ts) which electrically disconnects the amplifier from the first and second lines, and wherein the switch electrically disconnects the amplifier from the

second bit line when the potential of the second line is controlled to the third potential. wherein the switch electrically disconnects the amplifier from the first and second lines when the potential of the second bit line is controlled to the third potential, and wherein the amplifier is shared among the first and second lines and third and fourth bit lines different from first and second bit lines (Column 10, lines 60-67).

Regarding claims 14-16, the apparatus discussed above would perform the claim method 14-16.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai V. Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2827

THONG LE
PRIMARY EXAMINER